

## **REMARKS**

### **Rejections Under 35 USC § 102(e)**

Claims 1 - 21 have all been previously presented and arguments have been made to establish their distinctiveness with respect to the Cole patent.

In the office action, claims 1-2, 5-14 and 16-20 were rejected under 35 USC § 102(e) as being anticipated by United States Patent Number 6,654,523 to Cole. In light of the amendments made to independent claims 1 and 13 in the prior filed response, the before mentioned rejections of claims 1-2, 5-14 and 16-20 is respectfully traversed. The Applicant would like to point out that claim 21 was added as a new claim in the Applicant's response to the Office Action mailed November 3, 2005. It was not covered, and thus it appears not examined, in the latest Office Action mailed April 21, 2006. The Applicant would like to point out what makes claim 21 allowable over the prior art.

The Examiner has given a very broad interpretation to an "optical processing area." However, to one skilled in the art an optical processing area of an optical integrated circuit or planar lightwave circuit is an area in which an optical function is performed on an optical signal of interest. To one skilled in the art, an example list of optical functions includes: multiplexing, demultiplexing, interleaving, deinterleaving, filtering, attenuation, detection, dispersion compensation, polarization beam splitting, polarization rotation, switching, splitting, combining, optical signal add/drop as well as optical via and

optical delay functions.

The Applicant would like to point out in Figs. 1 and 2 that the optical processing area 24 is bordered by the integrated optical waveguides 25, 31 thus the integrated optical waveguides 25, 31 go "around" the optical processing area.

The Applicant respectfully disagrees with certain statements recited in the Office Action. That is, in support of the rejections, it was stated:

Whether the structure goes around in a loop with a small radius or large, it appears the limitations as currently claimed have been met by Cole. Finally, Cole discloses in Column 8, lines 20-25, any different loop configurations can be used as is known in the art (See US 6,122,423 for such a loop type structure as is known in the art).

Column 8, lines 20-25 of Cole recites:

Although the loop type alignment guides illustrated and described above are located near one or both of the outermost ends of the OIC waveguide rows, other positioning of the alignment guides is contemplated as falling within the scope of the present invention.

Thereafter, Cole describes other positioning of the alignment guides, such as those disclosed in Figures 7, 8 and 9. However, the structural limitations discussed below in claims 1, 13 and 21 are noticeably absent from the various examples specified in Cole and it is respectfully submitted that Cole's optical integrated circuit would not be easily modifiable to meet these structural limitations without severe modifications. For example, based on the teachings

of Cole, how would one modify Cole's alignment guides to have "an input and an output located on the first side with at least one of the waveguide ports between the input and the output of the waveguide structure" (as recited in independent claim 21)?

More particularly, claim 1 recites the step of "providing an integrated optical waveguide circuit component having an optical processing area, N input and output waveguide ports and at least one waveguide structure, the at least one waveguide structure going around the optical processing area." Claim 13, has been amended to recite the step of "providing an integrated optical waveguide circuit component having a first side, an optical processing area, N waveguide ports located on the first side, and at least one waveguide structure, the at least one waveguide structure having an input and an output located on the first side, with the input positioned near an end of the first side, and the output positioned near an opposite end of the first side".

Claim 21 recites the step of "providing an integrated optical waveguide circuit component having a first side, N waveguide ports located on the first side, and at least one waveguide structure, the at least one waveguide structure having an input and an output located on the first side with at least one of the waveguide ports between the input and the output of the waveguide structure."

As the Examiner is aware, a rejection under 35 USC § 102(e) requires

that each and every feature of the claimed invention be provided in a single prior art reference. With respect to "optical processing areas," Cole teaches in column 4, lines 61-65 that "the OIC 8 further includes an optical circuit 18, such as a *switching* or *multitplexing* circuit, which ... output waveguides 14." Cole further teaches in column 8, lines 54-5 that "the optical circuit 118 can be any type of optical circuit, for example, such as a modulating, *switching*, or *multiplexing* circuit. Cole describes an optical circuit 18, 118 (considered the optical processing area) having one or more alignment guides 150, 152, 154, and 156 (see for example the abstract and Fig. 2). However, Cole does not teach, or even suggest an integrated optical waveguide circuit component having at least one waveguide structure with the at least one waveguide structure going *around* the optical processing area (as recited in independent claim 1), or an integrated optical waveguide circuit component having a waveguide structure with the at least one waveguide structure having an input and output located on the first side, with the input positioned near an end of the first side, and the output positioned near an opposite end of the first side (as recited in independent claim 13). Additionally, the Cole reference does not teach, or even suggest an integrated optical waveguide circuit component having a first side, N waveguide ports located on the first side, and at least one waveguide structure, the at least one waveguide structure having an input and an output located on the first side with at least one of the waveguide ports

between the input and the output of the waveguide structure (as recited in independent claim 21).

Therefore, it is respectfully submitted that Cole does not teach each and every feature recited in independent claims 1, 13, and 21 and thus each of the claims that depend therefrom. In light of the foregoing, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 1-2, 5-14 and 16-20 in view of Cole.

### **Rejections Under 35 USC § 103(a)**

Claims 3-4 and 15 were rejected under 35 USC § 103(a) as being unpatentable over Cole as applied to claim 1 above. However, as discussed above, Cole does not teach the step of providing an integrated optical waveguide circuit component having an optical processing area, N input and output waveguide ports and at least one waveguide structure, the at least one waveguide structure going around the optical processing area as recited in claims 3-4, nor does Cole disclose the step of providing an integrated optical waveguide circuit component having a first side, an optical processing area, N waveguide ports located on the first side, and at least one waveguide structure, the at least one waveguide structure having an input and output located on the first side, with the input positioned near an end of the first side, and the output positioned near an opposite end of the first side as recited in claim 15.

Therefore, Cole does not teach or suggest the inventive concepts recited in claims 3-4 and 15, as amended.

Moreover, it is believed that MPEP §2143.01 supports the patentability of claims 3-4 and 15. That is, MPEP, §2143.01 states "The Prior Art must Suggest the Desirability of the Claimed Invention." In this case, Cole does not even mention the present invention recited in claims 3-4 and 15, much less suggest their desirability. For this reason alone, it is Applicant's belief that the subject matter of claims 3-4 and 15 is neither taught nor suggested.

Therefore, reconsideration and withdrawal of the rejection of claims 3-4 and 15 is respectfully requested.

### **CONCLUSION**

This is intended to be a complete response to the Office Action mailed April 21, 2006. Applicants respectfully submit that each and every rejection of the claims has been overcome, and that the claims as currently presented are in a condition for allowance. Favorable action is respectfully solicited.

Should the Examiner have any questions or comments concerning this response or the remarks contained herein, Applicants' attorney would welcome the opportunity to discuss such matters with the Examiner.

Respectfully submitted,



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